Claims

What is claimed is:

1. Method for reducing a crest factor of a multi-tone-data signal which is transmitted in a predetermined transmission frequency band ΔF, wherein a multi-tone-correction signal is substracted from said multi-tone-data signal, said multi-tone correction signal comprising a plurality of tone signals having frequencies outside said transmission frequency band ΔF.

2. Method for reducing a crest factor of a multi-tone-data signal according to claim 1 comprising the following steps:

(a) storing in a first memory at least one data symbol of a data symbol sequence, each data symbol comprising a predetermined number of data samples s(i) with index i, $0 <= i <= (N-1)$,

(b) comparing the amplitude of each data sample of said data symbol with a first threshold value to detect a data sample peak;

(c) performing the following steps when a data sample peak is detected;

(i) reading a multi-tone-correction signal comprising a corresponding number of correction data samples from a second memory;

(ii) shifting cyclically the read correction data samples of the multi-tone correction signal so that the maximum of said correction data samples coincides with the detected data sample peak;

(iii) scaling of the shifted correction data samples of the multi-tone-correction

signal according to a predetermined spectrum mask;

(iv) accumulating the scaled correction data samples of the multi-tone-correction signal in a third memory;

(d) subtracting the accumulated correction data samples of the multi-tone-correction signal from the data samples of said data symbol.

3. Method according to claim 2, wherein the amplitude of each data sample s(i) of said data symbol is compared with the first threshold value and the corresponding neighboured data samples s(i-m) and s(i+m) are compared with a second threshold value to detect a data sample peak with a high main and a high side amplitude.

4. Method according to claim 3, wherein when a data sample peak with a high main and a high side amplitude is detected at least one single tone-correction signal comprising a tone signal having a frequency within said transmission frequency band ΔF is subtracted from said multi-tone-data signal.

5. Method according to claim 2, wherein the amplitude of each data sample s(i) of said data symbol is compared with a thired threshold value and the corresponding neighboured data samples s(i-m) and s(i+m) are compared with the second threshold value to detect a data sample peak with a very high main and a high side amplitude.

6. Method according to claim 5, wherein when a data sample peak with a very high and a high side amplitude is detected, the multi-tone-correction signal comprising a plurality of tone signals having frequencies outside said transmission frequency band, and at least one signal tone-correction signal comprising a tone signal

having a frequency within said transmission frequency band ΔF are subtracted from said multi-tone-data signal.

7. Method according to claim 2, wherein said first threshold value, said second threshold value and said third threshold value are adjusted.

8. Method according to claim 2, wherein that third threshold value is higher than said first threshold value.

9. Method according to claim 2, wherein said second threshold value is lower than said first threshold value.

10. Method according to claim 1, wherein said multi-tone-data signal comprises a plurality of tone-signals having frequencies which are equidistant.

11. Method according to claim 1, wherein said multi-tone-data signal is a DMT (Discrete-Multi-tone Transmission) signal.

12. Method according to claim 1, wherein the multi-tone-data signal is an ADSL-signal.

13. A crest factor reduction circuit for reducing a crest factor of a multi-tone-data signal which is transmitted in a predetermined transmission frequency band ΔF, wherein the crest factor reduction circuit comprises means for subtracting a multi-tone-correction signal from said multi-tone-data signal, wherein the multi-tone-correction signal comprises a plurality of tone signals having frequencies outside said transmission frequency band ΔF.

14. Crest factor reduction circuit according to claim 13, wherein the crest factor reduction circuit has a data input for receiving a data symbol sequence of a data transmission signal.

15. Crest factor reduction circuit according to claim 14, wherein a first memory is provided for storing at least one data symbol of the received data symbol sequence, each data symbol comprising a predetermined number of data samples.

16. Crest factor reduction circuit according to claim 15, wherein the crest factor reduction circuit comprises a first comparator for comparing the amplitudes of each data sample s(i) of the stored data symbol with a first threshold value to detect a data sample peak.

17. Crest factor reduction circuit according to claim 16, wherein the crest factor reduction circuit comprises a Counter-Modulo-N which controls a multiplexer for switching sequentially the data samples to the first comparator.

18. Crest factor reduction circuit according to claim 13, wherein a second memory is provided for storing at least one multi-tone-correction signal comprising correction data samples, wherein the number of correction data samples corresponds to the number of data samples of a data symbol.

19. Crest factor reduction circuit according to claim 18, wherein a shifting unit is provided for shifting the correction data samples read from said second memory so that the maximum of the correction data samples coincides with the detected data sample peak.

20. Crest factor reduction circuit according to claim 19, wherein a scaling unit is provided for scaling the shifted correction data samples according to a predetermined spectrum mask.

21. Crest factor reduction circuit according to claim 20, wherein an accumulating unit is provided for accumulating the scaled correction data samples in a third memory.

22. Crest factor reduction circuit according to claim 21, wherein a subtractor is provided for subtracting the accumulated correction data samples from said data samples of the said received data symbol.

23. Crest factor reduction circuit according to claim 13, wherein a delay unit is provided for delaying the received data samples with a predetermined delay time.

24. Crest factor reduction circuit according to claim 21, wherein the third memory is reset by an overflow signal of said modulo-N-counter.

25. Crest factor reduction circuit according to claim 13, wherein the crest factor reduction circuit comprises a data output for outputting the corrected data samples as a sequence of corrected data symbols each comprising a predetermined number of corrected data samples.

26. Crest factor reduction circuit according to claim 25, wherein the data output of the crest factor reduction circuit is connected to a transmission signal path comprising:

(a) a digital filter for forming a digital transmission signal,

(b) a digital analog converter for converting the digital transmission signal into an analog transmission signal, and

(c) an analog filter for forming the analog transmission signal and a line driver for amplifying the analog transmission signal.

27. Crest factor reduction circuit according to claim 26, wherein the crest factor reduction circuit further comprises a convoluting unit for convoluting the received data samples with the impulse response of the transmission signal path.

28. Crest factor reduction circuit according to claim 15, wherein the crest factor reduction circuit comprises the first comparator for comparing the amplitudes of each data sample s(i) of the stored data symbol with the first threshold value and further comprises a second comparator for comparing the amplitudes of the corresponding neighboured data samples s(i-m) and s(i+m) with a second threshold value to detect a data sample peak with a high main and a high side amplitude.

29. Crest factor reduction circuit according to claim 15, wherein the crest factor reduction circuit comprises a third comparator for comparing the amplitudes of each data sample s(i) of the stored data symbol with the third threshold value and further comprises the second comparator for comparing the amplitudes of the corresponding neighboured data samples s(i-m) and s(i+m) with the second threshold value to detect a data sample peak with a very high main and a high side amplitude.

30. Crest factor reduction circuit according to claim 18, wherein the second memory further stores at least one single tone correction signal, wherein the single

tone-correction signal comprises a tone-signal having a frequency within the transmission frequency band.

31. Crest factor reduction circuit according to claims 28 and 30, wherein the single tone-correction signal is read from said second memory and supplied to the shifting unit when the first comparator and the second comparator detect a data sample peak with a high main and a high side amplitude.

32. Crest factor reduction circuit according to claim 28, wherein the multi-tone-correction signal and the single tone-correction signal are read from said second memory and supplied to the shifting unit when the third comparator and the second comparator detect a data sample peak with a very high main and a high side amplitude.

33. Crest factor reduction circuit according to claim 15, wherein the first memory is a RAM (Random Access Memory).

34. Crest factor reduction circuit according to claim 18, wherein the second memory is a RAM (Random Access Memory).

35. Crest factor reduction circuit according to claim 21, wherein the third memory is a RAM (Random Access Memory).

36. A transceiver for transceiving a data signal comprising:

(a) a coding unit for generating a multi-tone-signal from a received data bit stream;

(b) a IFFT unit for performing an inverse fast fourier transformation to generate a multi-

tone-data signal comprising a sequence of data symbols, each having a predetermined number (N) of data samples s(i) with index i, 0<= i <=(N-1);

(c) a crest factor reduction circuit for reducing a crest factor of the multi-tone-data signal which is transmitted in a predetermined transmission frequency band, wherein the crest factor reduction circuit comprises means for subtracting a multi-tone-correction signal from said multi-tone-data signal, wherein the multi-tone-correction signal comprises a plurality of tone signals having frequencies outside said transmission frequency band; and

(d) a transmission signal path for forming an analog transmission signal from the corrected multi-tone-data signal.

37. Transceiver according to claim 36, wherein the transmission signal path comprises a digital filter for forming a digital data transmission signal, a digital analog converter for converting the output signal of the digital filter into an analog signal, a analog filter for forming a analog transmission signal and a driving circuit for amplifying the analog transmission signal.

38. Transceiver according to claim 36, wherein the transceiver comprises a reception signal path.

39. Transceiver according to claim 38, wherein the reception signal path comprises an analog filter for limiting the frequency band of a received analog signal, an analog digital converter for converting the received analog signal into a digital signal and a digital filter for forming the received converted digital signal.

40. Transceiver according to claim 36, wherein an echo cancellation unit is provided for compensating echo signals.

41. Transceiver according to claim 40, wherein a subtractor is provided for subtracting the output signal of the echo compensating unit from the output signal of the reception signal path.

42. Transceiver according to claim 41,wherein a FFT-unit is provided for performing a fast fourier transformation of the output signal of the subtractor.

43. Transceiver according to claim 42, wherein a decoding unit is connected to the FFT-unit for performing a multi-tone demodulation.

44. Transceiver according to claims 36 and 39, wherein a hybrid circuit is provided which is connected to the output of the transmission signal path and to the input of the reception signal path.

45. Transceiver according to claim 36, wherein the transceiver is an ADSL-transceiver.